

SAND99-0591C

Back-Contact Crystalline-Silicon Solar Cells and Modules

James M. Gee, David D. Smith, Stephen E. Garrett,
Michel D. Bode, and Juan C. Jimeno*

Sandia National Laboratories⁺, Albuquerque, NM

**Universidad del País Vasco, Bilbao, Spain*

Abstract. This paper summarizes recent progress in the development of back-contact crystalline-silicon (c-Si) solar cells and modules at Sandia National Laboratories. Back-contact cells have potentially improved efficiencies through the elimination of grid obscuration and allow for significant simplifications in the module assembly process. Optimization of the process sequence has improved the efficiency of our back-contact cell ("emitter wrap through") from around 12% to near 17% in the past 12 months. In addition, recent theoretical work has elucidated the device physics of emitter wrap-through cells. Finally, improvements in the assembly process using back-contact cells are described.

INTRODUCTION

While a wide variety of semiconductor materials have been examined and are still currently under development for photovoltaic (PV) modules, the dominant technology today still uses bulk crystalline-silicon (c-Si) substrates. This dominant technology typically uses screen-printed metal gridlines on the front surface, which can shade up to 10 % of the active cell area. In the module assembly process, these cells are series connected by soldering tabs from the front of one cell to the back of another cell. This process requires multiple steps that are difficult to automate.

BACK-CONTACT CELLS

An alternative to the conventional process is made possible by the use of back-contact solar cells. The back-contact cell can have a higher efficiency than a front-contact cell due to elimination of grid obscuration losses, and has the potential to simplify the module assembly process.¹ Due to these potential advantages, there is presently considerable interest in back-contact silicon solar cells.²

⁺ Sandia National Laboratories is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under Contract DE-AC04-94AL8500.

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, make any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

We are developing the Emitter Wrap-Through cell (EWT). This back-contact cell structure has been described previously.³ The EWT solar cell has a phosphorus-diffused junction on the front and back surfaces. The phosphorus diffusion is either removed or masked from a small area on the back surface for the p-type contact. The front junction is electrically connected to the rear junction through laser drilled holes in the wafer, which are also phosphorus diffused. Interdigitated negative and positive grids are applied on the backside. Internal collection efficiency is high in this device due to the double-sided collection. Diffusion length requirements are only half that of a conventional front contacted solar cell to obtain similar collection efficiency.

Process Development

In the past year, improvements in the cell fabrication process have led to an efficiency improvement from 11.6% to 16.4%. Improvements have been made in plating, emitter passivation, and p-type surface passivation. We use photolithography for patterning the phosphorus diffusion and contacts in our laboratory prototypes. The starting material is typically 0.4- Ω cm float-zone silicon. The fabrication process has been described previously.³

Shunt conductance was a common defect in the early development of the EWT cell. The shunts were frequently due to bridging of the p-type and n-type contacts during the silver plating process. Slower plating rates and optimization of the plating bath chemistry have essentially eliminated shunt defects caused by the plating process.

Emitter surface recombination was minimized by retaining the oxide grown during the phosphorus diffusion. This oxide was grown to the proper thickness for use as an antireflection coating. In order to retain this oxide during the etching of the contact windows, a double-sided photolithography process was developed. Use of the emitter oxide produced a gain in short-circuit current of about 10 % due to enhanced blue response. The next variation on this process will involve stripping of the diffusion oxide, regrowth of a 10-nm passivation oxide, and deposition of a double-layer antireflection coating. This process will produce an antireflection coating optimized for use in a module.

We also added a boron-doped oxide to our EWT cell process. The mask oxide is deposited by APCVD and is patterned by photolithography. The mask oxide acts as a barrier to phosphorous diffusion as well as simultaneously diffusing a p⁺ layer at the p-type surface during the phosphorus emitter diffusion. As yet, the process is not optimized and only small gains in short-circuit current are observed by use of the boron-doped mask oxide as compared to an undoped mask oxide.

The EWT cell efficiency is currently limited by a low fill factor (FF). The low FF can not be attributed to either series resistance or shunt conductance. The poor FF manifests itself as a non-ideal diode characteristic near the maximum-power

point. A representative I-V curve is shown in Figure 1. The unusual aspect of this characteristic is that it only appears when the front side is illuminated. I-V characteristics are nearly ideal when illuminated from the back, gridded side, or in the dark.

Modeling

Other research groups have frequently observed a low FF in EWT-like back-contact cells. Recent papers have attributed the low FF to either a surface conductance channel between the rear emitter and the p-type contact, or to the large perimeter of exposed pn junction due to the interdigitated grid structure.²

We have developed a model for the EWT cell to help explain the low FFs that advances a new mechanism. Most of the EWT cell has a bipolar transistor (n^+pn^+) structure. In the nomenclature of transistors, the front n^+ diffusion is the emitter, the p-type bulk is the base, and the rear n^+ junction is the collector. Ideally, the diffused holes should electrically connect the emitter and collector with a low resistance. In this ideal case, photocurrent reaches the rear contacts by two paths – diffusion of minority carriers to the rear junction, or diffusion of minority carriers to the front junction and conduction through the holes. This ideal cell would have an I-V characteristic similar to an ideal diode.

Transistor effects will appear if the hole resistance is high. In this case, conduction of current through the holes biases the emitter with respect to the collector. Biasing of the emitter causes the emitter to inject minority carriers into the cell base, which can then be collected by the collector through the transistor effect. Since the current collected by the emitter is now bias dependent, the illuminated I-V curve shows apparent non-ideal behavior. In the extreme case of a floating front junction, the I-V curve will revert back to ideal behavior, but with a reduced short-circuit current since current collection now only occurs at the rear surface.

Very little current flows through the holes when the rear (gridded) surface is illuminated, and non-ideal behavior is not observed.

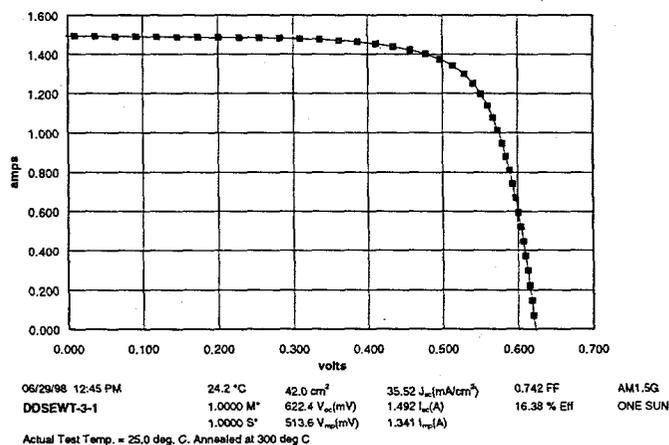
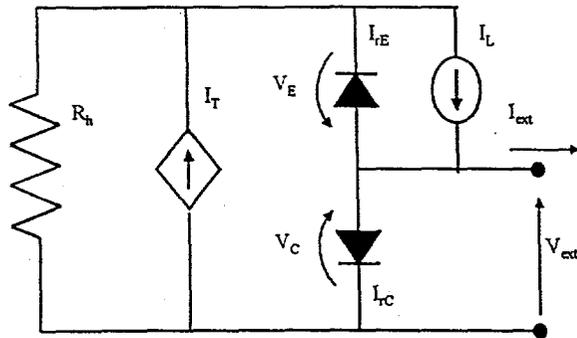


FIGURE 1. Representative one-sun IV curve of EWT cell.



The equivalent circuit of an EWT cell that includes the transistor effect is shown in Figure 2. The two diode currents, I_{rE} , and I_{rC} , represent the emitter and collector (i.e., front and rear n^+ junctions). I_L is the photogenerated current, R_h is the emitter and hole resistance, and I_T is the transistor current. Results of the

equivalent-circuit model have been compared to numerical simulations using PC1D, and excellent agreement between the models was obtained.

Two important parameters in the model are the hole resistance and the transistor current gain, β . These parameters can be estimated for EWT cells by fitting the illuminated I-V curve to the equivalent-circuit model, while the diode

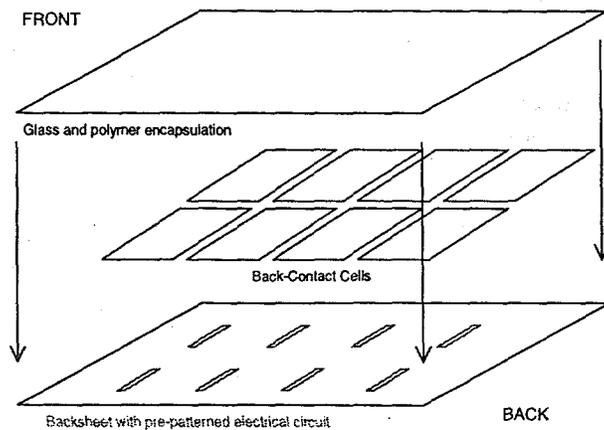
parameters are estimated from fitting of the dark I-V curve. For the device shown in Fig. 1, the fitted parameters are $R_h=7 \Omega\text{cm}^2$ and $\beta=10$. The expected hole resistance from a $35 \Omega/\text{sq}$, $70\text{-}\mu\text{m}$ diameter hole, and $300\text{-}\mu\text{m}$ cell, is $R_h=0.6 \Omega\text{cm}^2$.

FIGURE 2. Equivalent circuit of EWT cell using the Ebers Moll transistor model.

The model describes the I-V characteristics extremely well. However, the cause for the factor of ten discrepancy between calculated and expected R_h is unknown. One possibility is that the diffusion inside the hole is lighter than expected. The phosphorous diffusion is a gas source, and it is possible the dopant gasses do not penetrate to the interior of the hole as effectively as an exposed surface. Another possibility is a discontinuous diffused layer due to topographical features inside the hole. Experimental work is underway to directly measure the hole resistance and confirm the device model.

MONOLITHIC MODULE ASSEMBLY

The most significant advantage of the back-contact configuration is simplification of the module assembly.¹ The present geometry with contacts on front and back surfaces is difficult to automate and module fabrication (including labor and materials) now accounts for nearly 50% of the finished module cost. We are working on a new module assembly concept that encapsulates and electrically connects *all* the cells in the module *in a single step*. The key features of this new process include the following: (1) back-contact cells; (2) a module backplane that has both the electrical circuit and encapsulation material in a single piece; and (3) a single-step process for assembly of these components into a module (Fig. 3). This process reduces costs by reducing the number of steps, by eliminating low-



throughput (e.g., individual cell tabbing, cell stringing, layout, etc.) steps, and by using completely planar processes that are easy to automate. We refer to this process as “monolithic module assembly” since it translates many of the advantages of monolithic module construction of thin-film PV to wafered c-Si PV. Simplifications in the module fabrication have been

estimated to reduce the cost of module fabrication by up to 50%, which corresponds to a reduction of around 25% in the total manufacturing cost for the module.¹

FIGURE 3. Schematic illustration of monolithic module assembly.

We have previously described a process using conductive epoxy for the electrical attachment material.¹ The electrical resistance of the epoxy bonds continuously increased during thermal cycling, which led us to examine other materials for the electrical attachment. We are presently examining solder for the electrical attachment. Solder can make reliable, low-cost electrical attachments. However, we had to examine solders with relatively low liquidus temperatures (<150°C) due to the use of ethylene vinyl acetate (EVA) for the encapsulant.

We are examining bismuth-alloy solders with liquidus temperatures of 100 and 138°C. We were able to make electrical bonds with both solders during an encapsulation cycle in a standard pressure-vacuum laminator and using EVA. Metallography of assembled modules found that the solder joint was not continuous (Fig. 4). The EVA both melts and flows during the lamination cycle, which could interfere with wetting of the solder between the tinned copper electrodes and the solar cell buss bar. Changes in the geometry of the solder joint, stabilization of the copper electrode, and/or variations in the encapsulation process may improve the quality of the solder joints.

Thermal cycling of assembled modules is in progress. Modules using both bismuth-alloy solders are being cycled as well as some modules constructed with industry-standard Sn/Pb (63/37) solder. The cells were

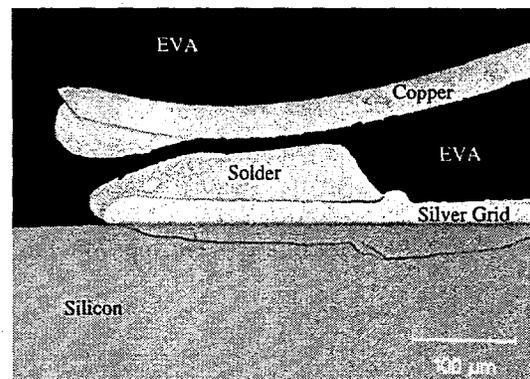


FIGURE 4. Metallograph cross section of bismuth-alloy solder bond in MMA module.

soldered prior to encapsulation in the modules using Sn/Pb solder similar to current industrial practice. The modules have 4 mechanical cells in series. The resistance of the series was monitored during thermal cycles of -40°C to $+90^{\circ}\text{C}$. The dwell times at the temperature extremes were 30 minutes each and the total cycle time is 3.5 hours.

Large changes in resistance were seen in one module using each of the bismuth alloys. This supports the results of the metallographic analysis that the solder joint is not continuous and probably not very strong. The other modules using the Bi-alloy solders and both of the Sn/Pb modules do not show any significant trends in the first 50 thermal cycles. Thermal cycling is planned to continue until at least 200 total cycles.

SUMMARY

There is resurgent interest in back-contact silicon solar cells due to its potential performance and module-assembly cost advantages. We reviewed our recent progress in back-contact cell and module development, which has included demonstration of 16.4%-efficient back-contact EWT cells, refinement of EWT device model, and improvement of the module assembly process.

ACKNOWLEDGEMENTS

B.L. Silva and J.W. Tingley assisted in the cell processing, J. Moore assisted in the device characterization, M.A. Quintana assisted in the module coring and metallography, and R.A. Ortiz assisted in the module assembly.

REFERENCES

1. Gee, J.M., *et al.*, "Simplified Module Assembly Using Back-Contact Silicon Solar Cells," 26th *IEEE Photo. Spec. Conf.*, pp. 1085-1088 (1996).
2. See, for example, the following papers from the 2nd *World Conf. on PV Energy Conv.*, Vienna, July 1998: Kress, A., *et al.*, "Low-Cost Back-Contact Silicon Solar Cells Applying The Emitter-Wrap Through (EWT) Concept"; Schönecker, A., *et al.*, "Attacking Limiting Factors In $10*10\text{ cm}^2$ Multicrystalline Silicon, Emitter Wrap-Through Solar Cell Design And Processing"; Van Kerschaver, E., *et al.*, "A Novel Silicon Solar Cell Structure with Both Polarity Contacts on the Back Surface"; and Roberts, S., *et al.*, "Interdigitated-Contact Solar Cells Made Without Photolithography".
3. Gee, J.M., *et al.*, "Emitter Wrap-Through Silicon Solar Cell," 23rd *IEEE Photo. Spec. Conf.*, pp. 265-270 (1993); and Gee, J.M., *et al.*, "Progress on the Emitter Wrap-Through Solar Cell," 12th *Eur. PV Solar Energy Conf.*, pp. 743-746 (1994).